1156. Effect of time delay on the pull-in range of phase locked loops

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Abstract. The pull-in range of phase locked loop (PLL) is a key parameter for evaluating the performance of the PLL circuit. It is defined as the maximum detuning frequency range where the loop locks. Different methods have been proposed for computing the pull-in range of phase locked loops in the absence of time delay. In this paper, the effect of time delay on the pull-in range of second-order phase locked loop as well as its dynamical behavior will be discussed. The time delay is modeled using first order Pade approximation. Using Pade approximation, the nonlinear second order delay differential equation which describes the phase error dynamic of the PLL is transformed into fourth order system in the state space representation. The new time-delay PLL model is simulated and different behavior is observed which is different than a typical PLL system without delay. As the gain of the loop increases, new behavior such as change of circuit stability and chaos are recognized which suggests that the gain of the loop cannot be arbitrary large. We compare the pull-in range of a time delay PLL with those without time delay. Results demonstrate the degradation in the pull-in range for the time delay PLL. Moreover, result shows that the pull in range gets narrower as time delay increases.

Keywords: phase locked loop, pull-in range, bifurcation, time delay, nonlinear differential equation.

1. Introduction

A phase-locked loop (PLL) is a feedback system that is used to maintain the phases of an output signal and a reference signal in a specific relationship. Phase-locked loops (PLL's) are used in many applications including frequency synthesis, demodulation, clock recovery and synchronization [1-3]. A PLL is used in a communication receiver to extract the modulated signal from a radio frequency carrier. This is accomplished by a PLL where the loop makes a voltage controlled oscillator (VCO) phase locking to the received input signal. The loop filter output will then contain the extracted FM signal, and the loop filter input will contain the PM signal. In this case the frequency response of the FM output will be a low-pass function described by the closed-loop transfer function and the PM output response will be a high-pass function described by the error function. In digital communications (modems) it is frequently necessary to extract a coherent clock signal from an input data stream. A PLL is often used for this task by locking a VCO to the input data and the data bits will be extracted from the input data by using the VCO output as a clock. Figure 1 shows the block diagram of the phase-locked loop (PLL) under investigation. It consists of three major parts: phase detector, VCO and low pass filter. The phase detector consists of a nonlinear device whose output is voltage proportional to the phase difference of the two input sinusoidal signals. The VCO is an electronic device that produces an output signal whose frequency is proportional to the input voltage. In this paper, we consider a second-order Type I PLL with sinusoidal phase detector characteristics. The PLL is driven by a sinusoidal signal with constant frequency of ω_i rad/sec, and the phase of the voltage controlled oscillator (VCO) is denoted as θ_v. The VCO's instantaneous frequency is equal to $\omega_o + K_v e$, where ω_o and K_v denote the VCO's free running frequency and gain, respectively. The analog multiplier produces an error signal that is proportional to $\sin(\varphi)$, where $\varphi \equiv \theta_i - \theta_v$ represents the closed loop phase error. The Loop filter is a low pass filter which processes the error signal and generates voltage e which drives the VCO in an attempt to make φ small and hence control the PLL dynamics. The dynamical model of this PLL is developed in Section 2. The quantities $G \equiv AK_1K_v$ and

$\omega_{os} \equiv \omega_i - \omega_o$ are a loop gain factor and the loop detuning, respectively and both of these parameters are assumed to be positive.

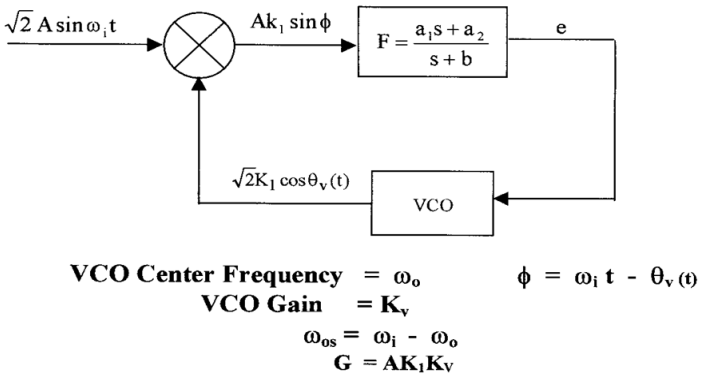


Fig. 1. Second order phase locked loop

There are key parameters that specify the operation of a PLL such as damping factor which is a measure of the ability of the PLL to track an input signal step. Usually it is used to indicate the amount of overshoot present in the output to a step perturbation in the input. Loop gain is the combination of all DC gains in the PLL which is usually can be expressed as the product of two values. The first one is the phase detector gain which is the ratio of the DC output voltage of the phase detector to the input phase difference and has the unit of volts/radian. The second one is the VCO gain which is the ratio of the VCO output frequency to the DC control input level and has the unit of radians/second/volt. Other key parameters in the PLL design are the capture range, lock-in range, pull-out range and pull-in range. These parameters specify the frequency ranges in which the PLL can operate. Capture range is defined as the range of input frequencies over which the PLL can acquire phase lock (hold range). Lock-in range is defined as the range of input frequencies over which the PLL will remain in phase lock once acquisition has occurred. Pull-out range is defined as the dynamic limit for stable operation of PLL. Pull-in range is defined as the range that the PLL will always be locked. When it is locked, the dynamics obey mostly linear theory, and it is analyzed traditionally by using the transfer function. However, when it is out-of-lock or when it is in the process of locking, the dynamics become nonlinear and the various phenomena inherent to nonlinear systems such as complex bifurcations and chaos can occur in phase-locked loops [4] and analysis becomes fairly difficult.

Extensive work has been conducted for analyzing the pull-in range and the dynamical behavior of classical phase locked loops without time delay. These include harmonic balance technique, the phase plane method and numerical analysis [5-7]. The problem of determining the pull-in range of phase locked loops is solved indirectly by evaluating the limit cycles of the loop in which the frequency error has a constant average. Harb and Stensby [8] developed a Galerkin based algorithm for computing the PLL's half-plane pull-in range. Piqueira et al. [9, 10] analyzed the effect of the double-frequency term and phase jitter in the operation of the nonlinear second-order phase-locked loop (PLL). Through numerical simulations, they confirm the dependence of oscillation on the PLL gain. Later, Piqueira [11] determined the lock in range for a third-order PLL analytically by identifying saddle-node and Hopf bifurcations. The work by Harb and Harb [13] showed that a third-order phase-locked loop (PLL) with sinusoidal phase detector characteristics experienced a Hopf bifurcation point as well as chaotic behavior. Later, they designed a nonlinear controller based on the theory of backstepping to control the chaotic behavior of the PLL [14]. On the other hand, Bradley and Straub [15] used chaos to broaden the capture range of phase locked loop. In the work of Endo et al. [16], chaos from PLL based frequency modulators was reported in the condition when the carrier frequency of the FM signal was outside

the locked state of the PLL.

Time delay is an unavoidable in certain applications of phase locked loops such as in the case of radio reception. Recently, many studies have been carried out to under-stand the causes of dynamic instabilities in phase locked loops. Time delay which is considered lumped in the predetection IF amplifier and/or a radio frequency interference rejection filter at the VCO output is found to be a major factor that causes dynamic instability in PLL. Analysis of nonlinear systems with time delays is extended from the knowledge available for standard nonlinear systems without delays and using some methods to approximate the delay like the Pade approximation method and harmonics approximation. Schanz and Pelster [17] proved the existence of a Hopf bifurcation in first order PLL with time delay using the method of multiple scale. Buckwalter and York [18] found an optimal gain that minimize the acquisition time for time-delay high frequency phase locked loop. Grant et al. [19] investigates the performance of optical phase-locked loops in the presence of non negligible loop propagation delay.

Time delay can generate instabilities in a PLL under certain gain and frequency detuning conditions. Consequently, the effect of time-delay on pull-in and hold-in range is a design constraint. The results of [18] indicate that increasing the loop gain improves both the pull-in and hold-in ranges for a second order phase locked loop. However, in this paper, analysis demonstrates that gain cannot be arbitrarily large to guarantee the pull-in process. This paper motivation is to highlight fundamentally different dynamical behavior in a second-order PLL due to loop time delay than is typically presented and how this time delay affect the pull-in range of the PLL under consideration. The analysis of the PLL is based on circuit parameters such as gain, time delay, poles and zeros of the filter and frequency detuning. Pade approximation will be used to approximate the time delay component in deriving the state space representation of a second-order phase locked loop with sinusoidal phase detector characteristics.

The paper is organized as follows: Section 2 illustrates the derivation and analysis of the PLL under consideration without time delay. Section 3 contains the dynamical model and derivation of state space representation of second order PLL with time delay. Simulation of the delay model and results will be presented in Section 4. In section 5 conclusions are drawn based on the analysis of the simulations.

2. Analysis of second-order PLL without delay

The PLL model depicted in Figure 1 has a closed loop phase error φ which satisfies:

$$\frac{d^2\varphi}{dt^2} + (b + G\cos\varphi)\frac{d\varphi}{dt} + a_2 G\sin\varphi = b\,\omega_{os}, \tag{1}$$

where φ is a function of time [7]. G and ω_{os} are assumed to be positive and $a_1 = 1$.

Define the two state variables $x_1(t)$, $x_2(t)$ as:

$$\begin{aligned} x_1 &= \varphi, \\ x_2 &= \dot{\varphi}. \end{aligned} \tag{2}$$

Eq. (1) can be written in state space representation as:

$$\begin{aligned} \dot{x}_1 &= x_2, \\ \dot{x}_2 &= -bx_2 - G\cos(x_1)\,x_2 - a_2 G\sin x_1 + b\omega_{os}. \end{aligned} \tag{3}$$

The desired behavior of the second order PLL is phase locking. Mathematically, this behavior corresponds to solutions such that $\dot{x}_1 = 0$ and $\dot{x}_2 = 0$. Solving Eq. (3) we get the equilibrium points given by:

$$X_{eq} = \begin{bmatrix} \pi - \sin^{-1}\left(\frac{b\omega_{os}}{a_2 G}\right) - 2\pi k \\ 0 \end{bmatrix}. \quad (4)$$

The eigenvalues of the Jacobian matrix determine the local stability of the equilibrium points. The Jacobian matrix associated with the second order PLL is determined to be:

$$J = \begin{bmatrix} 0 & 1 \\ G\sin(x_1)\, x_2 - a_2 G\cos(x_1) & -b - G\cos(x_1) \end{bmatrix}. \quad (5)$$

Evaluating the Jacobian matrix at the equilibrium point given by Eq. (4) yields:

$$J = \begin{bmatrix} 0 & 1 \\ -a_2 G\cos(x_1) & -b - G\cos(x_1) \end{bmatrix}, \quad (6)$$

and the corresponding characteristic equation is given by:

$$\lambda^2 + \lambda\big(b + G\cos(x_1)\big) + a_2 G\cos(x_1) = 0. \quad (7)$$

It is was verified that for values of $0 < \omega_{os} < \frac{a_2}{G}$, Eq. (7) has two eigenvalues of opposite sign which indicates that the equilibrium point is a saddle type and hence a separatrix cycle (saddle-to-saddle connection) exists. The PLL under consideration is in phase-locked when the phase error φ is constant, and a stable equilibrium condition exists. It is well known that phase lock is possible (but may not be achieved when the loop is closed) for [7, 8]:

$$\omega_{os} < \omega_h = AK_1K_v a_2 b \equiv G\frac{a_2}{b}. \quad (8)$$

The frequency ω_h is known as the PLL's hold in range. Finally, no stable equilibrium points exist, and phase lock is cannot happen for $\omega_{os} > \omega_h$. Under condition (8), it is known that the PLL's state vector $\left[\varphi \ \frac{d\varphi}{dt}\right]$ must approach (as $t \to \infty$) a stable limit cycle with:

$$\varphi(t;\omega_{os}) = \omega_f(\omega_{os})t + \psi(t;\omega_{os}), \quad (9)$$

where ψ is periodic function with fundamental frequency of ω_f [8]. This limit cycle is known as a stable false lock state [7]. This state corresponds to a periodic solution of the nonlinear differential equation describing the PLL. The PLL's pull-in range ω_p is one of the main parameters in practical applications of phase locked loops. As positive ω_{os} decreases, a point $\omega_{os} = \omega_p$, $\omega_h > \omega_p > 0$, is reached where $\varphi(t;\omega_{os})$ bifurcates, and phase lock occurs. No false lock state (limit cycles) exist for $0 \le \omega_{os} < \omega_p$, and the PLL will pull in (i.e., achieve phase lock) regardless of the initial conditions when the loop is closed. This is based on the fact that a separatrix cycle terminates the PLL's stable limit cycle associated with the false lock state as detuning parameter ω_{os} decreases through the pull-in value ω_p (bifurcation point). Figure 2 is a typical phase plane plot which indicates the case where $\varphi(t;\omega_{os})$ bifurcates directly from an externally stable separatrix cycle (dark line). The plot was computed for a PLL containing a loop filter with $a_1 = 1$, $a_2 = 100$ and $b = 10$. Note that $x = \varphi$ and $y = \frac{d\varphi}{dt}$.

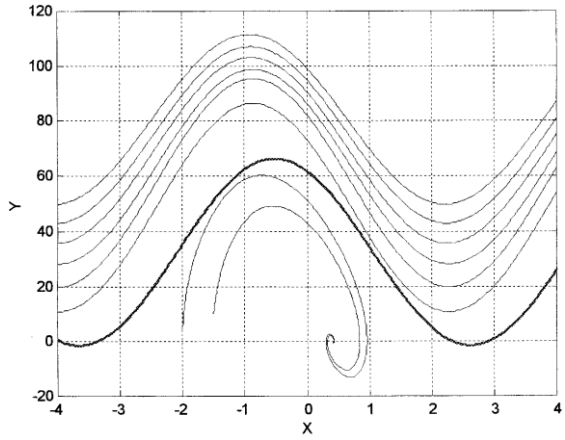
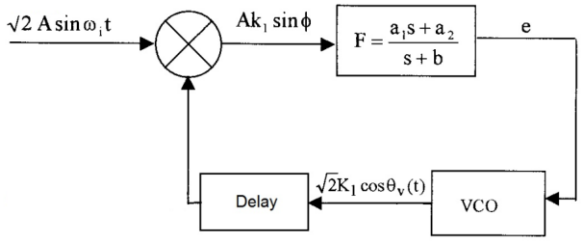


Fig. 2. Bifurcation of a limit cycle from a separatrix cycle (dark line) as ω_{os} decreases

3. Derivation and analysis of the PLL with delay

Consider Figure (3) which represents the block diagram for second-order delay phase-locked loop.



VCO Center Frequency $= \omega_o$ $\qquad \phi = \omega_i t - \theta_{v(t)}$

VCO Gain $= K_v$

$\omega_{os} = \omega_i - \omega_o$

$G = AK_1K_V$

Fig. 3. Second order delay phase locked loop

The equation of the second order system with feedback time delay is given by:

$$\frac{d^2\varphi}{dt^2} + b\frac{d\varphi}{dt} + G\cos\varphi(t-\tau)\frac{d\varphi}{dt}(t-\tau) + a_2 G\sin\varphi(t-\tau) = b\omega_{os}. \tag{10}$$

Define the four state variables $x_1(t)$, $x_2(t)$, $x_3(t)$ and $x_4(t)$ as:

$$\begin{aligned} x_1 &= \varphi, \\ x_2 &= \dot{\varphi}, \\ x_3 &= x_1(t-\tau), \\ x_4 &= x_2(t-\tau). \end{aligned} \tag{11}$$

In order to write the above equations in state space representation, the first order Pade approximation will be used for the delay operator. Note that Eq. (11) can be written as:

$$\begin{aligned} \dot{x}_1 &= x_2, \\ \dot{x}_3 &= x_4. \end{aligned} \tag{12}$$

Substitute these state variables in Eq. (10) to get:

$$\dot{x}_2 = -bx_2 - G\cos(x_3)\,x_4 - a_2 G\sin(x_3) + b\,\omega_{os}. \tag{13}$$

By using the first order Pade approximation [20]:

$$e^{-s\tau} = \frac{1 - s\tau/2}{1 + s\tau/2}. \tag{14}$$

We obtain:

$$\begin{aligned} \dot{x}_3 &= \frac{2}{\tau}(x_1 - x_3) - x_2, \\ \dot{x}_4 &= \frac{2}{\tau}(x_2 - x_4) - \dot{x}_2. \end{aligned} \tag{15}$$

Substitute Eq. (13) into Eq. (15) to get:

$$\dot{x}_4 = \frac{2}{\tau}(x_2 - x_4) + bx_2 + G\cos(x_3)\,x_4 + a_2 G\sin(x_3) - b\,\omega_{os}\,. \tag{16}$$

It is obvious now that the time delay inherent in the PLL doubles the system order and the second order system becomes a fourth order system. The state space representation of the second order PLL with delay is given by:

$$\begin{aligned} \dot{x}_1 &= x_2, \\ \dot{x}_2 &= -bx_2 - G\cos(x_3)\,x_4 - a_2 G\sin(x_3) + b\omega_{os}, \\ \dot{x}_3 &= x_4, \\ \dot{x}_4 &= \frac{2}{\tau}(x_2 - x_4) + bx_2 + G\cos(x_3)\,x_4 + a_2 G\sin(x_3) - b\omega_{os}. \end{aligned} \tag{17}$$

The equilibrium point is given by setting $\dot{x}_1 = \dot{x}_2 = \dot{x}_3 = \dot{x}_4 = 0$ in Eq. (17). By doing so, one obtains:

$$x_{eq} = \begin{bmatrix} \sin^{-1}\left(\dfrac{b\omega_{os}}{a_2 G}\right) \\ 0 \\ \sin^{-1}\left(\dfrac{b\omega_{os}}{a_2 G}\right) \\ 0 \end{bmatrix}. \tag{18}$$

The local stability of the system can be checked based on the Jacobian matrix given by:

$$J = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & -b & J_{23} & -G\cos(x_3) \\ 0 & 0 & 0 & 1 \\ 0 & b + \dfrac{2}{\tau} & J_{43} & J_{44} \end{bmatrix}, \tag{19}$$

where $J_{23} = Gx_4\sin x_3 - aG\cos(x_3)$, $J_{43} = -J_{23}$, $J_{44} = -\frac{2}{\tau} + G\cos(x_3)$.

Substitute $x_1 = x_3 = \sin^{-1}(b\omega_{os}/a_2 G)$ and $x_2 = x_4 = 0$ to evaluate the Jacobian matrix around the equilibrium point to get:

$$J = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & -b & J_{23} & -G\cos(x_3) \\ 0 & 0 & 0 & 1 \\ 0 & b + \dfrac{2}{\tau} & J_{43} & J_{44} \end{bmatrix}. \tag{20}$$

Define the constant:

$$\beta = \cos(\sin^{-1}(x)) = \sqrt{1 - x^2} = \sqrt{1 - \left(\frac{b\omega_{os}}{aG}\right)^2}. \tag{21}$$

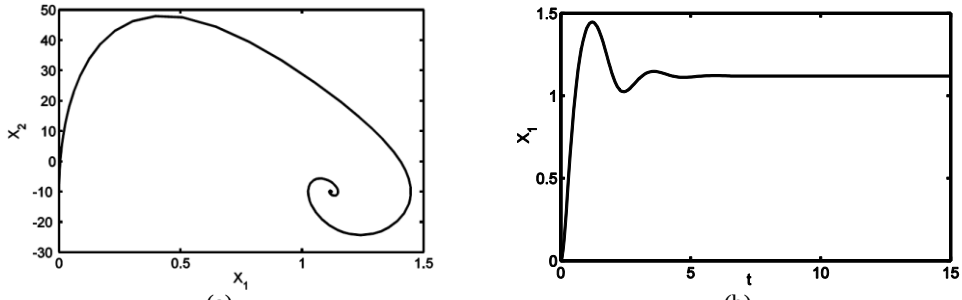
Solve det $(J - \lambda I) = 0$ to get the following characteristics equation:

$$\lambda^3 + A\lambda^2 + B\lambda + C = 0, \tag{22}$$

where $A = 2/\tau + b - \beta G$, $B = \frac{2b + 2G\beta}{\tau} - a_2 G\beta$, $C = 2a_2\beta G/\tau$.

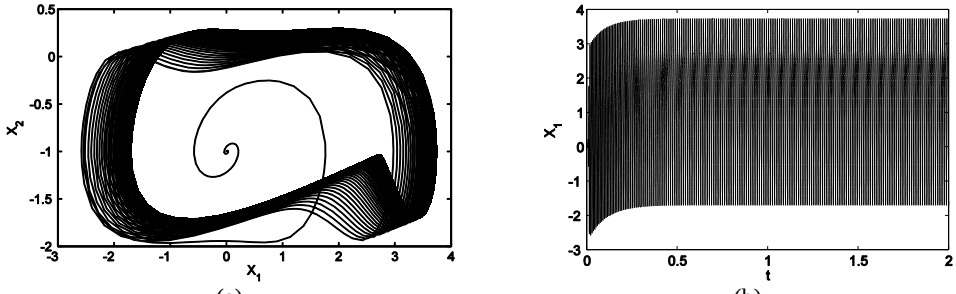
4. Simulation of the delay model

The system given by Eq. (17) is simulated using MATLAB fixed value of time delay ($\tau = 0.002$) and different values of gain. The values of $a_1 = 1$, $a_2 = 100$ and $b = 10$ are fixed throughout the simulation. Figure (4) shows that the system is in phase lock state for $G = 100$ K. Increasing in G, the system exhibits a chaotic behavior as shown in Figure (5). This behavior starts at $G = 20$ K and the system remains in this regime up to $G = 60$ K. This range is wider than that in the first order PLL [17] which makes it more efficient to be used as chaos generator.



(a) (b)

Fig. 4. (a) Phase plane trajectory (equilibrium solution) for $G = 100$ K and $\tau = 0.002$ sec; (b) time domain history for $G = 100$ K and $\tau = 0.002$ sec



(a) (b)

Fig. 5. (a) Phase plane diagram (chaotic behavior) for $G = 60$ K and $\tau = 0.002$ sec; (b) time domain history for $G = 60$ K and $\tau = 0.002$ sec

In order to study the effect of time delay on the pull-in range, Eq. (17) is simulated for different values of delay and gain. For a fixed values of delay (τ) and gain (G), the pull-in range is determined by finding the value of ω_{os} – where the system given by Eq. (17) changes its stability from equilibrium state (phase-lock state) to a periodic solution (out-of-lock) state as ω_{os} changes. These results are summarized in Table (1) below. Figure (6) shows the pull-in range of a second-order phase locked loop without delay and with delays of 0.003 sec and 0.012 sec. The figure shows clearly the degradation in the pull-in range due to time delay. Furthermore, it demonstrates that as the time delay increased, the pull-in range gets narrower. For these plots, the values of $a_1 = 1$, $a_2 = 100$ and $b = 10$ are used.

Table 1. Gain versus the pull in range for different values of delay

G (Gain)	Pull in range No delay	Pull in range ($\tau = 0.003$ sec)	Pull in range ($\tau = 0.012$ sec)
5	24	23	23
20	91	89	82
30	137	134	120
40	183.5	179	158
50	231	225.5	193
60	279	272	229
70	328	319	264
80	377	367	300
100	474	466	365
120	573	565	425
130	624	616	460

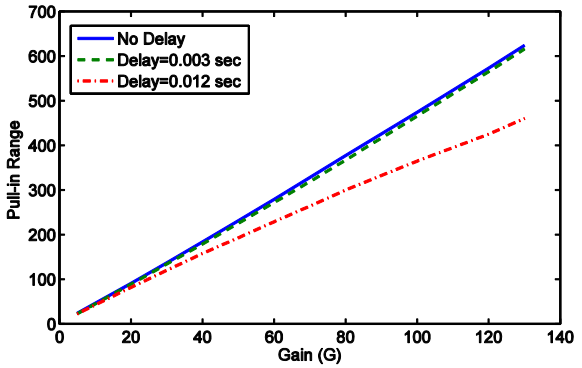


Fig. 6. Pull-in range vs. gain for second order phase locked loop

5. Conclusions

New results concerning the pull-in range of delay phase locked loop are reported. The effect of time delay on the pull-in range of second-order phase locked loop as well as its dynamical behavior are presented. First order Pade approximation is used to model the time delay element which is presented in the loop. By using Pade approximation, the nonlinear second order delay differential equation which describes the phase error dynamic of the PLL is transformed into fourth order system in the state space representation. This time-delay PLL model is simulated and different behavior is observed which is different than a typical PLL system without delay. As the gain of the loop increases, new behavior such as change of circuit stability and chaos are recognized which suggests that the gain of the loop cannot be arbitrary large. The pull-in range of a time delay PLL is compared with those without time delay. Results showed that the pull-in range for the time delay PLL is narrower than PLL without delay. Moreover, result shows that the pull in range gets narrower as time delay increases. Also, it is found that for delay phase locked loop

the degradation of the pull-in range becomes more noticeable as the closed loop gain increased and this needs to be investigated in future work.

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